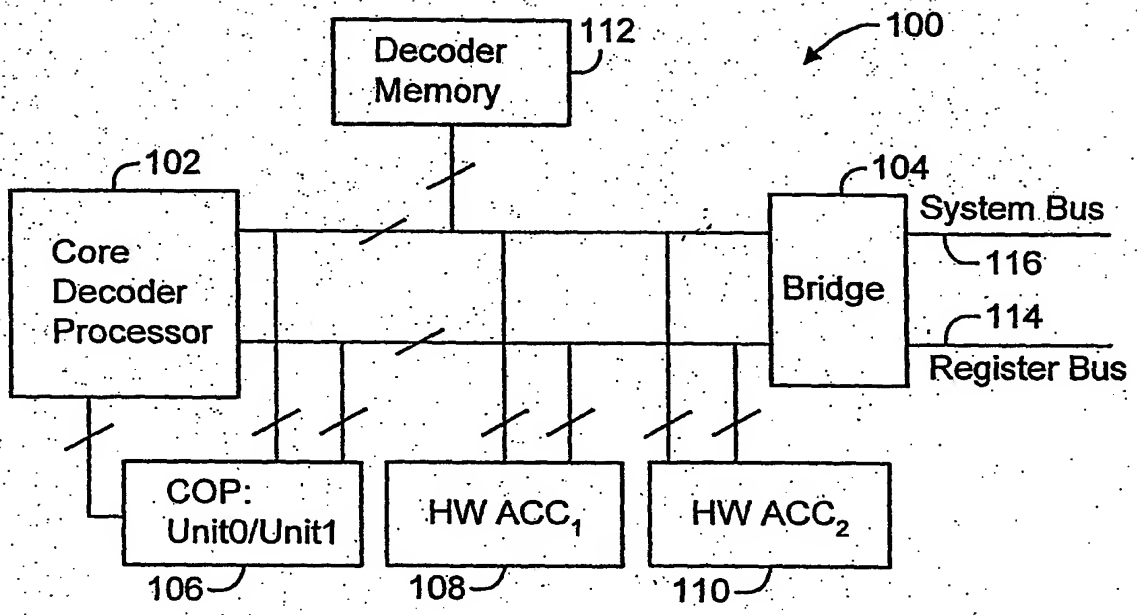
Decoder Memory
112
100
102
104
Core Decoder Processor
Bridge
System Bus
116
114
Register Bus
COP: Unit0/Unit1
HW ACC1
HW ACC2
106
108
110

FIG. 1

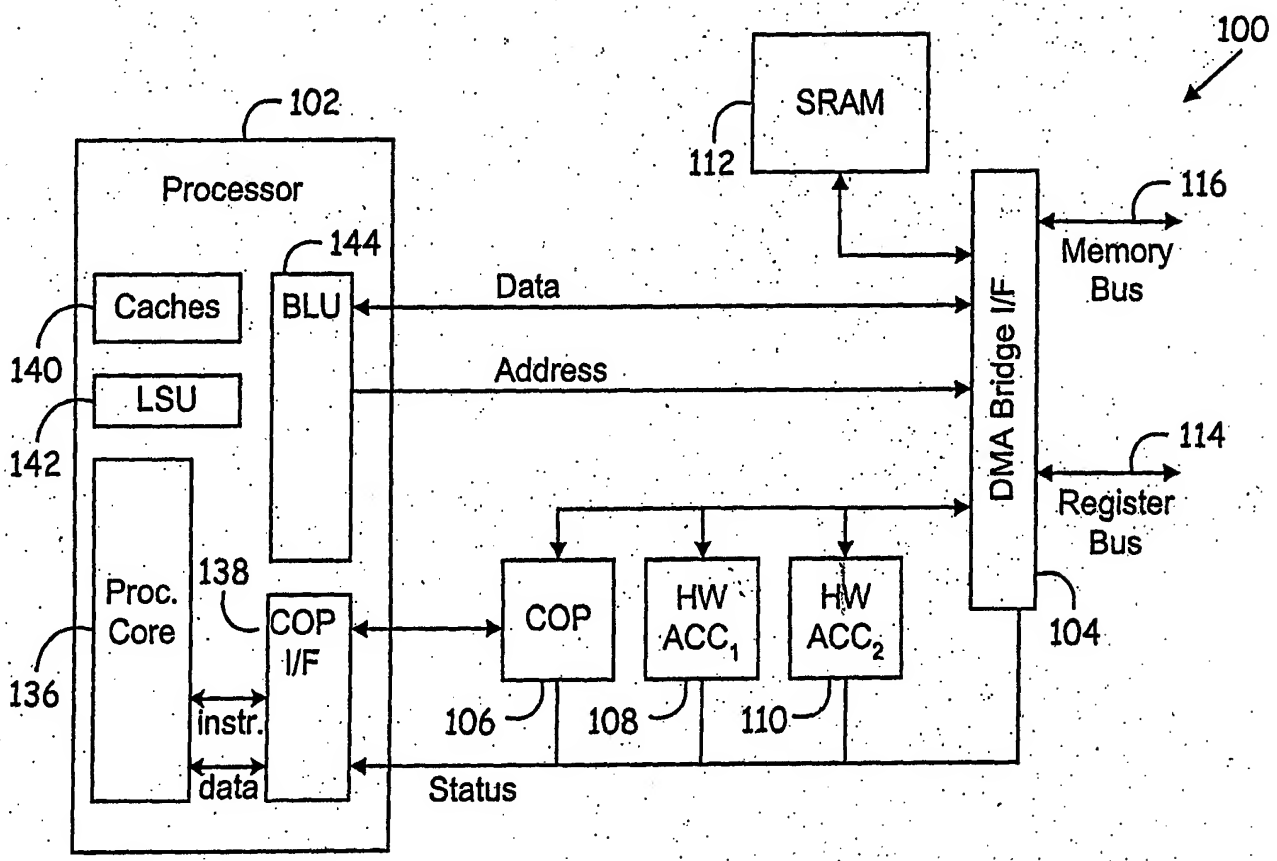
100
102
Processor
SRAM
112
116
Memory
Bus
144
Caches
BLU
Data
140
LSU
Address
142
DMA Bridge I/F
114
Register
Bus
Proc.
Core
138
COP
I/F
COP
HW
ACC1
HW
ACC2
104
136
instr.
data
106
108
110
Status

FIG. 2

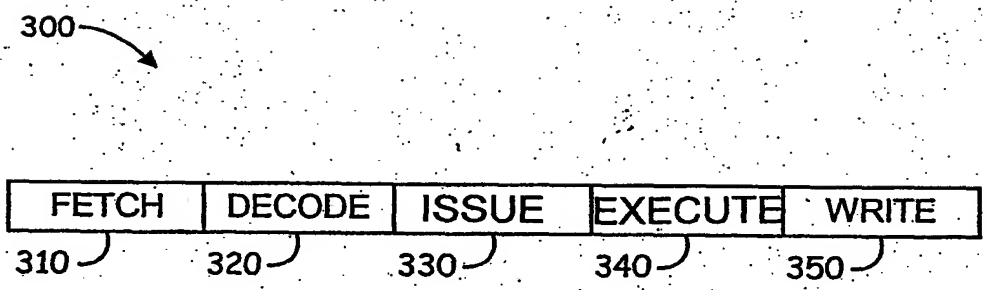

FIG. 3

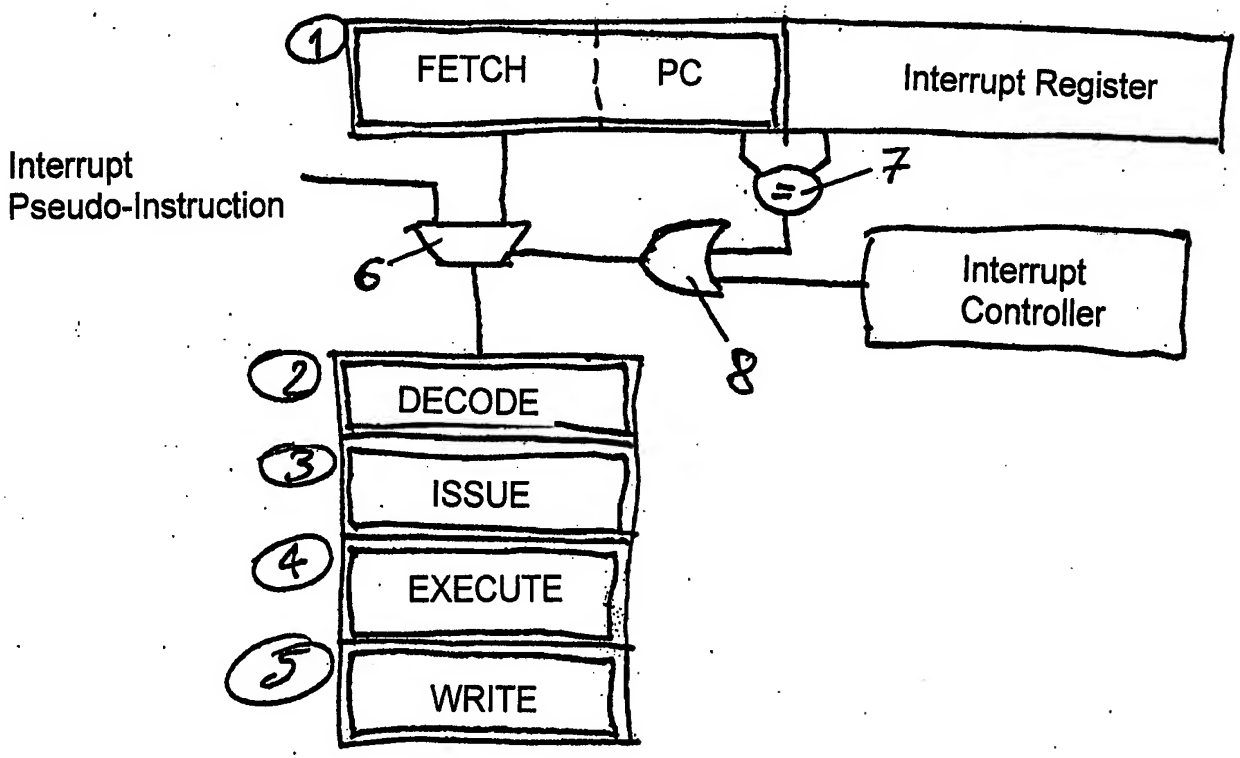
1
FETCH
PC
Interrupt Register
Interrupt
Pseudo-Instruction
7
=
6
8
Interrupt
Controller
2
DECODE
3
ISSUE
4
EXECUTE
5
WRITE

FIG. 4